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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/712,736
Filing Date: November 12, 2003
Appellant(s): CHEUNG ET AL.

Carlton H. Hoel (Reg. No. 29,934)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 2, 2006 appealing from the Office action mailed December 22, 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,816,996	Hill et al.	3-1989
5,047,927	Sowell et al.	9-1991

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim 7-11 are rejected under 35 U.S.C. 103(a) as obvious over Hill et at (US 4,816,996) in view of Sowell et al. (US 5,047,927) in the final office action mailed December 22, 2004.

Claim 7, Hill discloses an SPI (Fig. 3; col. 2, lines 44-46) having plurality of hardware pointers (56, 60) to memory locations in a FIFO buffer (RAM 36), one hardware counter (51), and a hardware logic device (30-34, 40-43, 49, 53) with bus interface (21, Fig. 2) to utilize the FIFO buffer for intermediate storage data transmitted from/to CPU (inherent function of SPI, see background: col. 1, lines 18-col. 2, line 8).

Hill discloses all the limitations of claim 7 except the use of a DMA for providing cycle stealing. Sowell discloses that it is well known to use DMA and its cycle stealing technique to reduce CPU overhead and support fast and efficient transfer of data. It would have been obvious to one having ordinary skill in the art to utilize DMA and its cycle stealing, as is taught by Sowell, with the SPI of Hill in order to improve data communication, reduce CPU overhead and provide efficient means of data movement (Sowell: col. 3, ll. 5-10).

Claim 8, Hill discloses the queue pointer providing SPI transmitter/receiving signals depending on the mode of transmission (col. 5, ll. 18-52).

Claim 9, Hill discloses the SPI having transmitter buffer and receiver buffer (input and output buffers 31-32; col. 3, lines 20-23) configured to receive/transmit data to the FIFO buffer (Fig. 3).

Claims 10-11, Hill discloses the SPI module configured to operate as one of master and slave (31-32, Fig. 3) and having data register chip select signal (37, FIG. 3) to the bus interface.

(10) Response to Argument

A) *Appellants argue that Hill does not disclose or suggest the presently claimed invention including the SPI being further configured to communicate with the DMA module and the bus interface for providing cycle stealing.*

It appears that Appellants argue that **Hill alone does not teach all the claim limitations**. The examiner agrees with appellants that Hill alone does not disclose the SPI for providing cycle stealing (i.e. Hill discloses the SPI for transfer of data, but does not disclose a DMA for providing cycle stealing). **Please note that the claims were rejected under 35 USC 103 (a) as obvious over Hill in view of Sowell.**

As indicated in the claim rejections, Hill discloses all the claimed limitations except for using a DMA with the SPI for providing cycle stealing (i.e. Hill discloses the SPI for transfer of data, but does not disclose a DMA for providing cycle stealing). Sowell teaches using DMA cycle stealing mode in order to provide a fast and efficient means for retrieving and placing data that is required for data movement. The examiner relies on the teaching of using DMA cycle stealing mode of Sowell with the SPI of Hill in order to enhance performance of the SPI (i.e. reduce CPU overhead and provide fast and efficient means of data movement). The DMA of Sowell, when employed with the SPI of Hill, would communicate with the SPI in order to transfer data efficiently. The examiner has therefore established that the combination of Hill and Sowell teaches all

the limitations of the claims with the motivation for combining the references, and therefore has set forth the prima facie case of obviousness for the combination of the references.

Appellant's arguments are **not persuasive** because they appear to be made **against the references individually (Hill only), and not against the combination of the references (Hill and Sowell)**. One cannot show patentability/nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

B) *Appellants further argue that Sowell does not disclose or suggest the presently claimed invention including the SPI being further configured to communicate with the DMA module and the bus interface for providing cycle stealing. Appellants acknowledge that Sowell discloses a direct memory access (DMA) providing a fast means for retrieving and placing data that is required for a HDLC block, and the DMA being generally used in a "cycle stealing mode" which provides an efficient means of data movement - then conclude that Sowell* ***or*** *any prior art reference applied by the Examiner does not disclose a SPI having cycle stealing.*

It is unclear what Appellants intend to argue by "*Sowell* ***or*** *any prior art reference applied by the Examiner does not disclose a SPI having cycle stealing".* It appears that Appellants argue that **Sowell alone does not teach all the claim limitations**, or **any prior art reference alone does not teach all the claim limitations**. The examiner agrees with appellants that Sowell alone (or any prior art reference alone) does not

disclose the SPI for providing cycle stealing. **Please note again that the claims were rejected under 35 USC 103 (a) as obvious over Hill in view of Sowell.**

As discussed above, the examiner has established that the combination of Hill and Sowell teaches all the limitations of the claims with the motivation for combining the references, and therefore has set forth the prima facie case of obviousness for the combination of the references.

Appellant's arguments are again **not persuasive** because they appear to be made **against the references individually (Sowell only), and not against the combination of the references (Hill and Sowell)**. One cannot show patentability/nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellants' conclusion that "*Sowell **or** any prior art reference applied by the Examiner does not disclose a SPI having cycle stealing" does not appear to be* a rebuttal regarding the combination of references or a rebuttal regarding the statement for obviousness being in error, and appellants have not made any rebuttal regarding the combination of references or any rebuttal regarding the statement for obviousness being in error anywhere else in the response.

Since Appellants have not made any other remark or rebuttal regarding the combination of references or the statement of obviousness, Appellants have **failed to**

properly and sufficiently provide evidence to overcome the prima facie case of obviousness.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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November 8, 2006